

Please add new claims as follows:

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39. A queue as claimed in Claim 11 wherein a packet vector stored in the second memory includes a link to a next packet vector in the queue.
40. A queuing method as claimed in Claim 19 wherein the cache row is transferred in a single write cycle.
41. A queuing method as claimed in Claim 23 wherein a packet vector stored in the second memory includes a link to a next packet vector.
42. A queue as claimed in Claim 36 wherein a packet vector stored in the second memory includes a link to a next packet vector in the queue.
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REMARKS

The specification has been amended to correct errors of a clerical nature. No new matter has been added.

Acceptance is respectfully requested.

Respectfully submitted,

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